Amendments to the Specification

Please replace paragraph 2 on page 1 with the following revised paragraph:

This application is related to the following copending applications, all of which are incorporated herein by reference: Serial No. 09/996,113, filed November 28, 2001, for "Unified Digital Architecture" (Docket No. RAL920010003US2); Serial No. 09/996,053, filed November 28, 2001, for "Analog Unidirectional Serial Link Architecture" (Docket No. RAL920010005US2); and Serial No. 09/997,587, filed November 28, 2001, for "Apparatus And Method For Oversampling With Evenly Spaced Samples" (~~Attorney~~ Docket No. RAL920010011US2).

Please replace paragraph 1 on page 6 with the following revised paragraph:

synchronous operation of the extraction of the bits from the register 24 by the selector 26 for delivery to the latches 28a and 28b. Also, the counter operates to form a synchronous delivery of the bits from the latches 28a and 28b to the multiplexor 30 and therefrom to the latch 32. It is at the driver equalizer 34 that the digital bits synchronously received are converted to a serial analog signal 35. The functioning and more detailed description of the various parts of the transmitter 16, such as the bit register 24, selector 26, the latches 28a and 28b, the multiplexor 30, the latch 32, the single phase, full rate, phase lock loop 36 and the counter 38 are all described in more detail in application Serial No. 09/996,113, filed November 28, 2001, for "Unified Digital Architecture" (Docket No. RAL920010003US2) and application Serial No. 09/996,053, filed November 28, 2001, for "Analog Unidirectional Serial Link Architecture" (Docket No. RAL920010005US2), which applications are incorporated herein by reference. The analog output 35 is placed on the serial bus 20. It is transmitted in an asynchronous form to the receiver 18 attached to the other end of the serial bus 20. As indicated above, the receiver 18 receives the asynchronous analog signal and converts it to a synchronous digital parallel signal corresponding to the digital bits in register 24 for storage in the receiver 18.

Please replace paragraph 1 on page 7 with the following revised paragraph:

detection and edge detection circuit 58 and a multi-phase, half rate phase loop lock 60. This technique operates by sampling, and preferably multiple sampling, both edges of the data in the analog signal and converts the data in the analog signal to parallel data bits. Preferably, the multiple samples are used to determine the approximate center point of each resulting data bit. This is an oversampling circuit which will convert the asynchronous analog serial signal in selector 62 to a digital output 63 in two-bit increments delivered to a shift register 64. A counter 66, which is actuated by the phase rotator 54, operates on shift register 64 to output the two-bit digital signals as ten-bit synchronous signals to ten-bit register 68. The operation of this receiver 18 is described in detail in application Serial No. 09/996,053, filed November 28, 2001, for "Analog Unidirectional Serial Link Architecture" (Docket No. RAL920010005US2), and application Serial No. 09/997,587, filed November 28, 2001, for "Apparatus and Method for Oversampling with Evenly Spaced Samples" (Docket No. RAL920010011US2), which applications are incorporated herein by reference.